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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
NGUYEN, PHUONGCHAU BA

ART UNIT	PAPER NUMBER
2665	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/228,445	FREITAG ET AL.	
	Examiner	Art Unit	
	Phuongchau Ba Nguyen	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *7-16-02 Amendment* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11 and 14-16* is/are rejected.

7)☒ Claim(s) *12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-11, 14-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kumar (5,970,069) in view of Rowett (5,991,817).

Regarding claim 11:

Kumar (5,970,069) discloses a method for transmitting and receiving a serial data stream including alternating portions of multiple serial data channels, comprising:

providing a plurality of functional units (SWAN 76, 4xSerial 80, E110 controller 74, V.34 IF 72) each configured to perform a specific function of a serial communication protocol upon the portions of the multiple serial data channels, wherein each functional unit is a state machine having a set of unique operating states (i.e. transmit and receive states; col.27, lines 2-14; col.27,

lines 27-32; col.25, lines 43-54 & 57-60), and wherein state information stored within a given functional unit determines the one of the unique operating states in which the functional unit is operating; and

(DMAC controller 82; col.22, lines 8-13) transferring state information between the plurality of functional units and a memory unit (DMAC Registers;col.25, lines 11-21) such that the plurality of functional units operates alternately upon the portions of the multiple serial data channels (the connections between the controllers 72, 74, 76 and MultiChannel DMA controller 82; col.22, lines 8-44).

Kumar does not explicitly disclose providing a plurality of functional units each configured to perform a specific function of a serial communication protocol upon the portions of the multiple serial data channels.

Rowett discloses in figure 11a that a Bbus time slot for assigning a timeslot to serial channels. Therefore, it would have been obvious to an artisan to implement Rowett's teaching into Kumar's system and the motivation being to maximize the bandwidth utilization if an available bandwidth (unused timeslot) is available on the channel {col.10, lines 34-45}.

Regarding claim 1:

Kumar (5,970,069) discloses a serial communication controller (MultiChannel DMA controller 82 in fig.3) for transmitting and receiving a serial data stream including multiple serial data channels having portions which alternate in time with respect to each other {by TSA col.29, lines 41-44}, comprising:

a plurality of functional units (controllers 72, 74, 76 in figure 3) operably coupled in series, wherein each functional unit is configured to perform a specific function of a serial communication protocol.

Kumar is different from the claim that the plurality of functional units in Kumar does not operate in time sequence upon the portions of the multiple serial data channels.

Rowett (5,991,817) discloses a time slot assigner TSA 46 (fig.1) which is coupled to multiple serial communication controller SCC 45 {col.4, lines 40-41}. TSA 46 would assign different time slots (portion of multiple serial data channels) to each functional units (controller SCC 45){col.11, lines 60-62}, thus each functional units (controller SCC 45) would operate in a time sequence

corresponding to the assigned different time slots (e.g., the different time slots are 1, 2, 3...n-1; col.10, lines 34-40; col.11, lines 3-6, wherein DMAC services the channel assigned to each time slot in order 0-15—in sequence).

Therefore, it would have been obvious to a skilled artisan to couple the TSA 46 as taught by Rowett to the controllers (72, 74, 76) in Kumar's system, the motivation being to disassemble data packets located in different time slots in a multiplexed data stream to different controllers (72, 74, 76) using different protocols{col.11, lines 60-62; col.14, lines 48-49} thus improving router performance in processing different types of data in of the network in a avoiding congestion.

Regarding claim 2: The serial data stream includes digital data of only one of the multiple serial data channels at any given time, and wherein each of the multiple serial data channels is assigned a periodically recurring time segment and is active during its assigned time segment, and wherein the plurality of functional units operates upon the active serial data channel {Rowett, col.11, lines 60-62}.

Regarding claim 3: Each functional unit (72, 74, 76 in Kumar) is a state machine having a set of unique operating states (read on the time slot assigned to controllers for when to transmit on bus by TSA 46 in Rowett) and wherein each functional unit (72, 74, 76 in Kumar) comprises a set of memory elements (buffers or registers; col.27, lines 2-14; col.27, lines 27-32; col.25, lines 43-54 & 57-60 in Kumar), and wherein state information (read on the assigned transmit time slot from TSA 46, Rowett) stored (by receiving the assigned time slot from TSA 46, Rowett) within the set of memory elements of a given functional unit determines the one of the unique operating states in which the functional unit is operating (in Rowett, the assigned time slot from TSA 46 would be used for determining the unique time when a controller is allowed to transmit) {col.4, lines 37-39; col.9, lines 34-37; col.11, lines 60-62, Rowett}.

Regarding claim 4: Kumar further discloses a memory unit (SRAM 84) operably coupled to each of the plurality of functional units, wherein the memory unit includes a separate portion (link list; fig.24; col.8, lines 1-29, Kumar) allocated

to each of the multiple serial data channels for storing the state information of the functional units (col.24, lines 16-20; Kumar).

Regarding claim 5: Kumar further discloses a microcontroller (CPU 90) coupled to each of the plurality of functional units and to the memory unit, wherein the microcontroller transfers state information between the functional units (72, 74, 76) and the memory unit (SRAM 84) such that the plurality of functional units operates alternately upon the portions of the multiple serial data channels {fig.3}.

Regarding claim 6:

Kumar discloses in figure 3 a serial communication controller for transmitting and receiving a serial data stream including alternating portions of multiple serial data channels, comprising:

a plurality of functional units (72, 74, 76) each configured to perform a specific function of a serial communication protocol, and wherein each

functional unit comprises a programmable state register (buffers or registers; col.27, lines 2-14; col.27, lines 27-32; col.25, lines 43-54 & 57-60 in Kumar);

a memory unit (SRAM 84) including a separate portion (link list; fig.24; col.8, lines 1-29, Kumar) allocated to each of the multiple serial data channels for storing the state information of the functional units {col.24, lines 16-20; Kumar}; and

a microcontroller (CPU 90) coupled to each of the plurality of functional units (72, 74, 76) and to the memory unit (SRAM 84), wherein the microcontroller is configured to transfer state information between the plurality of functional units and the memory unit such that the plurality of functional units operates alternately upon the portions of the multiple serial data channels.

Kumar does not explicitly disclose that each functional unit having a set of unique operating states; and state information is stored within the state register of a given functional unit determines the one of the unique operating states in which the functional unit is operating;

Rowett (5,991,817) discloses a time slot assigner TSA 46 (fig.1) which is coupled to multiple serial communication controller SCC 45 {col.4, lines 40-41}.

Therefore, it would have been obvious to a skilled artisan to couple the TSA 46 as taught by Rowett to the controllers (72, 74, 76) in Kumar's system, the motivation being to disassemble data packets located in different time slots in a multiplexed data stream to different controllers (72, 74, 76) using different protocols{col.11, lines 60-62; col.14, lines 48-49}. Thus, the set of unique operating states read on the time slot assigned to controller (72, 74, 76) for when to transmit on the bus by TSA 46 in Rowett; and the state information (read on the assigned transmit time slot from TSA 46, Rowett) stored (by receiving the assigned time slot from TSA 46, Rowett) within the state register (which is read on the buffer or register in Kumar at each controllers 72, 74, 76) of any given functional unit determines the one of the unique operating states in which the functional unit is operating (in Rowett, the assigned time slot from TSA 46 would be used for determining a unique time for when a controller is allowed to transmit){col.4, lines 37-39; col.9, lines 34-37; col.11, lines 60-62, Rowett}.

Regarding claim 7: Rowett further discloses a time slot assigner group (TSA 46) coupled to the microcontroller (DMAC), wherein the time slot assigner group (TSA 46) includes clocking circuitry (143, 149; figs.16-17) and keeps track of which of the multiple serial data channels is active (in 145, 152, 141, 150).

Regarding claim 8: The time slot assigner group (TSA 46) produces an output signal (wherein the output signal read on assigned a time slot which is generated by TSA 46) indicating which of the multiple serial data channels is active, wherein the microcontroller (CPU 90) receives the output signal and performs the state information transfers in response to the output signal.

Regarding claim 9: Rowett further discloses that the time slot assigner group (TSA 46) includes an active time slot register (SCC register 146), and wherein the contents of the active time slot register indicate which of the multiple serial data channels is active, and wherein the microcontroller (CPU 90) reads the active time slot register and performs the state information transfers dependent upon the contents of the active time slot register.

Regarding claim 10:

Kumar and Rowett disclose the plurality of functional units (72, 74, 76; Kumar), the memory unit (SRAM 84; Kumar), the microcontroller (CPU 90; Kumar) and the time slot assigner group (TSA 46, Rowett).

Kumar and Rowett does not explicitly disclose that all memory unit, microcontroller, time slot assigner group are formed upon a single monolithic semiconductor substrate.

However, it is well known in the art to make integral of all memory unit, microcontroller, time slot assigner group upon a single monolithic semiconductor substrate {In re Larson, 144 USPQ 347 (CCPA 1965)}.

Regarding claim 14:

Kumar (5,970,069) discloses a serial communication system (fig.3), comprising:

an interface unit (2X TSM 78) adapted for coupling to a transmission medium 86, wherein the interface unit is configured to receive a receive serial data stream (from TDM serial I/F 42) and to provide the receive serial data

stream (transmit data to SWAN 76 which comprises clock recovery 312; col.5, lines 49-58);

a timing recovery unit (Clock Recovery & Generation 312 in SWAN 76) coupled to receive the receive serial data stream from the interface unit, wherein the timing recovery unit 312 is configured to produce a clock signal derived from the receive serial data stream and to provide the receive serial data stream; and

a serial communication controller (Multiple channel DMA controller 82) coupled to (the SWAN having Clock Recovery 312 for receiving) receive the clock signal and the receive serial data stream, wherein the serial communication controller 82 comprises a plurality of functional units (E110 Controller 74, V.34 IF 72, SWAN 76, SRAM 84, CW4011-MiniRISC 90) operably coupled in series, and wherein each functional unit is configured to perform a specific function of a serial communication protocol,

Kumar does not explicitly discloses that the plurality of functional units operates alternately upon the portions of the multiple serial data channels of the receive serial data stream.

Rowett (5,991,817) discloses a time slot assigner TSA 46 (fig.1) which is coupled to multiple serial communication controller SCC 45 {col.4, lines 40-41}.

Therefore, it would have been obvious to a skilled artisan to couple the TSA 46 as taught by Rowett to the controllers (72, 74, 76) in Kumar's system, the motivation being to disassemble data packets located in different time slots in a multiplexed data stream to different controllers (72, 74, 76) using different protocols{col.11, lines 60-62; col.14, lines 48-49}.

Regarding claim 15: Kumar further discloses that the serial communication controller (DMAC 82) is further configured to produce a transmit serial data stream including alternating portions of multiple serial data channels, and wherein the interface unit (2X TSM) is coupled to receive the transmit serial data stream and further configure to drive the transmit serial data stream upon the transmission medium {fig.3 in Kumar; fig.1 in Rowett}.

Regarding claim 16: Kumar further discloses that the serial communication controller (DMAC 82) is adapted for coupling to a host processor (CPU 90, fig.3 in Kumar).

Allowable Subject Matter

3. Claims 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed 7-16-02 have been fully considered but they are not persuasive.

A/. Applicant argued that Kumar and Rowett do not teach a serial communication controller including a plurality of functional units operably coupled in series. {remarks page 8}.

In reply, Kumar teaches each functional units 76, 74, 72 coupled in series with the serial controller 82 because, as well known in the art, at least two devices connected to each other over at each end of a channel/line is

considered as coupled in series, thus the controller 82 is coupled in series with each functional units 72, 74, 76 (it is noted that 72, 74, 76 are parallel to each other not to controller 82).

Claims 1-16 are rejected in combination of Kumar and Rowett. Thus, in response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the

advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuongchau Ba Nguyen whose telephone number is 703-305-0093. The examiner can normally be reached on Monday-Friday from 10:00 a.m. to 3:00 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on 703-308-6602. The fax phone numbers for the organization where this application or proceeding is assigned are 703-872-9314 for regular communications and 703-872-9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4700.

PN

Phuongchau Ba Nguyen
Examiner
Art Unit 2665

October 21, 2002

10/21/02